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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER
HUA, L

ART UNIT	PAPER NUMBER
	8

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

5/18/95

☑ This application has been examined ☑ Responsive to communication filed on Feb. 10, 1995 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474..
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1-62, and 63-94 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☑ Claims 1-62 have been cancelled.
3. ☑ Claims 70-94 and 95-97 are allowed.
4. ☑ Claims 63-69 and 70-78 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. Claims 64-~~77~~ 69 are rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim.

As per claims 64-69:

These dependent claims refer to the memory system card which is not the invention set forth in parent claim 63. Notice that the parent claim claims a memory system, not the memory system card.

2. Claim 67 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 67:

A lines 1-2, the phrase "said memory card" lacks antecedent basis.

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claim 63-~~69~~ 78 are rejected under 35 U.S.C. § 103 as being unpatentable over Nozawa et al. (4,525,839, hereafter referred to as Nozawa).

As per claim 63:

Nozawa discloses the feature of defective sector substitution in a memory system substantially as claimed. Nozawa's memory system is connectable to a computer system and comprises:

an array (elements 11T and 13T and the sectors therein) of non-volatile memory cells partitioned into a plurality of sectors(n, n+1, n+2, n+3, ...; sectors N, N+1, N+2, N+3, ...) and that individually include a distinct group of the array of memory cells;

means (elements 60 and 70) for controlling operation of the array;

means (pointers 23a) for linking any defective ones of the plurality of sectors to others of the sectors; and

means (elements 50, 51, 61, 64, 63, 71, 76 and 77; see also step 130 shown in figure 6 or step 222 of figure 8; and

column 14, lines 24) for accessing linked others of the sectors in place of the defective sectors.

However, Nozawa does not teach that his memory system cells are of floating gate type. But Nozawa teaches that his system is of disk drive storage system type.

It would have been obvious to an artisan at the time the invention was made to apply Nozawa's feature of defective sector substitution into a memory system of floating gate type.

The artisan would have been motivated to apply Nozawa's feature into a floating gate memory system of because the group of floating gate memory cells in the floating gate memory system are prone to be defective and different features of defective memory area substitution have been used for replacing a defective memory cells in the floating gate memory with an alternate memory area.

As per claim 64:

Nozawa's linking means (23a) is stored in the array.

As per claim 65:

Nozawa's accessing means is within the controller (elements 60 and 70).

As per claim 66:

Nozawa teaches that his memory system is accessible by read and write commands issued by channel 51 which is understood to be

connected to the processor to which the memory system is connected.

As per claim 67:

Nozawa teaches that his feature can be applied to a recording system where the data is processed as a block and that the recording medium is of disk type. (Column 7, lines 55-59).

As per claim 68:

Nozawa's sector linking means is a list of defect pointers which map defective sectors into one of the others of the sectors. (See column 3, line 22, to column 4, line 34).

As per claim 69:

The means for adding a defect pointer to a list for mapping a particular sector into another sector is inherent in the system of Nozawa in order for the system of Nozawa to record (into pointer section 23a) the sector position of the sector which has been too many number of defective cells such that the read error cannot be corrected by the error correction code. (See column 3, lines 55-59).

As per claims 70 and 71:

Nozawa discloses the invention substantially as claimed. Nozawa's teaches a method of operating a computer system, more specifically a method of re-mapping defective memory sector. Nozawa's method comprises the step of:

providing an array (elements 11T and 13T and the sectors therein) of non-volatile memory cells partitioned into a plurality of sectors(n, n+1, n+2, n+3, ...; sectors N, N+1, N+2, N+3, ...) and that individually include a distinct group of the array of memory cells;

providing means (elements 60 and 70) for controlling operation of the array;

identifying when a sector becomes defective (column 3, lines 55-59)

linking by the means (pointers 23a) for linking any defective ones of the plurality of sectors to others of the sectors; and

accessing by the means (elements 50, 51, 61, 64, 63, 71, 76 and 77; see also step 130 shown in figure 6 or step 222 of figure 8; and column 14, lines 24) for accessing linked others of the sectors in place of the defective sectors.

However, Nozawa does not teach that his memory system cells are of floating gate type. But Nozawa teaches that his system is of disk drive storage system type.

It would have been obvious to an artisan at the time the invention was made to apply Nozawa's feature of defective sector substitution into a memory system of floating gate type.

The artisan would have been motivated to apply Nozawa's feature into a floating gate memory system of because the group of floating gate memory cells in the floating gate memory system are prone to be defective and different features of defective memory area substitution have been used for replacing a defective memory cells in the floating gate memory with an alternate memory area.

As per claim 72:

Nozawa's linking means (23a) is stored in the array.

As per claim 73:

Nozawa's accessing means is within the controller (elements 60 and 70).

As per claim 74:

Nozawa teaches that his memory system is accessible by read and write commands issued by channel 51 which is understood to be connected to the processor to which the memory system is connected.

As per claim 75:

Identifying when a sector becomes detective by referencing to the number of defective cells such that the read error cannot be corrected by the error correction code is taught by Nozawa (see column 3, lines 55-59).

As per claim 76:

Nozawa teaches the storing of user data. The storing of overhead information would have been obvious to an artisan because Nozawa teaches storing information and overhead information is information which can be stored. The artisan would have been motivated to store the overhead information because the overhead information is informative.

As per claim 77:

Nozawa teaches the storing sector addresses in the individual sectors.

As per claim 78:

Nozawa teaches the storing of error correction codes.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly V. Hua whose telephone number is (703) 305-9684.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

L. Hua
April 14, 1995

ROBERT W. BEAUSOLIEL, JR.
SUPERVISORY PATENT EXAMINER
GROUP 2400